



Embedded Linux
Conference

Europe



OpenIoT Summit
Europe

Embedded Linux on RISC-V

Khem Raj

@himvis

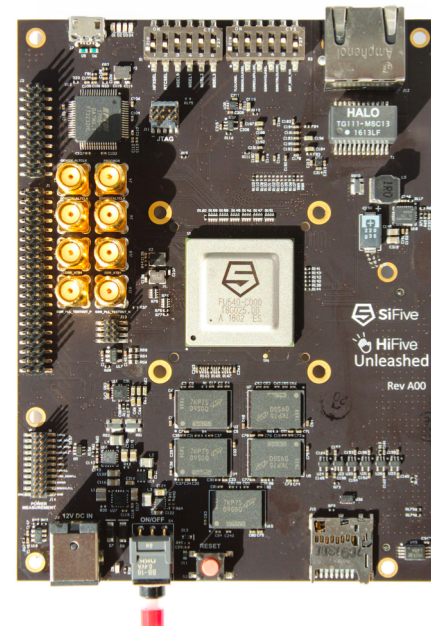


Agenda

- Introduction
- Upstream Status
- What works
- Work in progress
- Q/A

RISC-V (risk-five)

- “Fifth” RISC ISA from Berkeley
- 32, 64 and 128 bits wide instruction sets
- little-endian by default
- Specifications
 - <https://riscv.org/specifications/>
- RV32I and RV64I + Extensions
 - M - Integer Mult/Div
 - A - Atomic Memory access
 - F - Floating point (single precision)
 - D - Floating point (Double precision)
 - C - Compressed
- Concatenate to represent ISA
 - E.g. RV64IMAFD
 - ‘G’ is abbreviation for ‘IMAFD’
- RV64GC is generally supported ISA by major distros e.g. (Fedora, Debian, ...)
- Non-standard extensions begin with ‘X’
 - E.g. RV64GXargle_Xbargle



Tools

- Binutils – 2.28
- GCC – 7.0
- GLIBC – 2.27
 - Rv32i – 2.28
- Newlib – 3.0.0
- Qemu - 2.12.0
- GDB – 8.2
 - Baremetal support only
 - riscv*-*-elf

GNU Binutils 2.28 Released, Adds RISC-V Support

Written by [Michael Larabel](#) in [GNU](#) on 6 March 2017 at 11:18 AM EST. [2 Comments](#)



Binutils 2.28 is out today as the latest version of this important GNU package.

Binutils 2.28 brings new options (`--remove-relocations=SECTIONPATTERN` and `nm --with-version-strings`), improvements to the ARC and PowerPC ports, Gas adds support for the RISC-V architecture, Gas also now supports the Cortex-M23 and Cortex-M33 processors, and GNU ld also adds RISC-V support, and other new options. The RISC-V architecture support was also recently merged for the GCC 7 compiler stack.

RISC-V Port Lands In GCC 7 Codebase

Written by [Michael Larabel](#) in [GNU](#) on 6 February 2017 at 05:18 PM EST. [4 Comments](#)



Last month the [RISC-V GCC port](#) was approved for landing in GCC 7 while today that merge finally happened.

The RISC-V GCC port has been a work in progress for a long time and was [held up by university lawyers](#) while that was all cleared up, the code went through a few rounds of code revisions, and the steering committee approved landing RISC-V support even as the codebase has moved onto only bug/regression fixes. Today all of that code finally was merged into the GCC7 code-base.

[RISC-V SW Dev](#)

Newlib 3.0.0 released with RISC-V support

6 posts by 5 authors



Kito Cheng

★ Hi folks:

newlib 3.0 was released last week[1]. It's first official release with RISC-V support, you can find that in their ftp[2], and read more new changes from their NEWS file[3].

[1] <https://sourceware.org/newlib/2018/msg00019.html>

[2] <ftp://sourceware.org/pub/newlib/index.html>

[3] https://sourceware.org/git/gitweb.cgi?p=newlib-cygwin.git;a=blob_plain;f=newlib/NEWS;hb=HEAD

Boot Loaders

- Coreboot
 - Supports RISC-V upstream
- U-Boot – 2018.11
 - RISC-V virt board
 - Support is Upstream
- PK/BBL (Proxy Kernel/Berkeley Boot Loader)
 - <https://github.com/riscv/riscv-pk>



RISC-V Linux Kernel Port

- Stable ABI in upstream since 4.15
- 4.19 contains drivers for Qemu “virt” board
- Major Contributors



Berkeley
UNIVERSITY OF CALIFORNIA



SiFive



Operating Systems -Zephyr

- <https://docs.zephyrproject.org/latest/boards/riscv32/index.html>
 - SiFive HiFive1
 - Microsemi M2GL025 Mi-V
 - RISC-V32 Emulation (QEMU)
 - Zedboard Pulpino
- **Released in 1.13.0**
- Now Included in Standard SDK releases

Distribution Ports – cross-distro Defaults

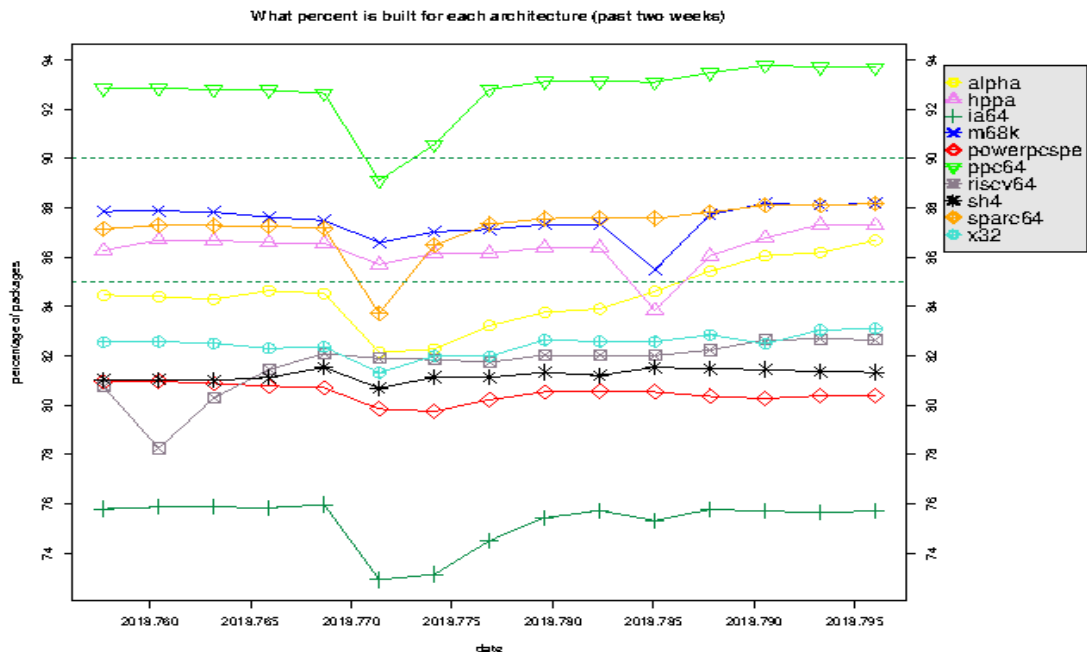
- Uses RV64GC - LP64 ABI
- Little-Endian
- Embedded Linux Distributions
 - Have RV32I ABI variants
 - More...

Operating Systems - Fedora

- <https://fedoraproject.org/wiki/Architectures/RISC-V>
- Instruction of installation:
- <https://fedoraproject.org/wiki/Architectures/RISC-V/Installing>
- Info about Bootstrapping and Building
 - Bootstrap finished in March'18
 - Koji build farm is up
 - Fedora 29/Rawhide packages building using koji
 - <http://fedora-riscv.tranquillity.se/koji/>
 - Self-hosted
 - HiFive Unleashed
 - QEMU

Operating Systems - Debian

- <https://wiki.debian.org/RISC-V>



OpenEmbedded/Yocto

- First RISC-V Linux Distro
 - <https://riscv.org/2015/01/a-linux-distribution-for-risc-v/>
 - Poky Fork (yocto Project Reference Distro)
- Core Support up-streamed - 2.5 release
- BSP/Architecture Layer - (meta-riscv)
 - <https://github.com/riscv/meta-riscv>
 - QEMU machine
 - SiFive Freedom U540
 - Application Development Cross SDK
 - On device SDK
 - Baremetal rv32 and rv64 targets
 - Generates bare-metal SDKs useful for RTOSes e.g. zephyr
- Current Tuning
 - RV32, RV64
- Continuous Integration
 - In progress
- World Builds
 - <http://errors.yoctoproject.org/Errors/Build/70151/>



38 errors for Build #70151

Edit columns ▾ Show rows: 25 ▾									
Submitted on ▼	Error type	Failure	Machine	Distro	Host distro	Branch	Commit	Similar	
21/10/18 14:29	Recipe	gststreamer1.0: do_compile	qemuriscv64	yoe	arch/arch	yoe/mut	b7c5ac5...	0	
21/10/18 14:29	Recipe	gststreamer: do_configure	qemuriscv64	yoe	arch/arch	yoe/mut	b7c5ac5...	3	
21/10/18 14:29	Recipe	rust-cross-riscv64: do_rust_gen_targets	qemuriscv64	yoe	arch/arch	yoe/mut	b7c5ac5...	0	
21/10/18 14:29	Recipe	python-greenlet: do_compile	qemuriscv64	yoe	arch/arch	yoe/mut	b7c5ac5...	4	
21/10/18 14:29	Recipe	libglt2-native: do_configure	qemuriscv64	yoe	arch/arch	yoe/mut	b7c5ac5...	0	

```
| NOTE: Ran 16 tests in 18.662s
| NOTE: FAILED
| NOTE: (failures=2, skipped=2)
| DEBUG: Stopping logging thread
| DEBUG: Stop event received
| DEBUG: Tearing down logging thread
| DEBUG: Sending SIGTERM to runqemu
| RESULTS:
| RESULTS - connman.ConnmanTest.test_connmand_help - Testcase 961: PASSED (0.31s)
| RESULTS - connman.ConnmanTest.test_connmand_running - Testcase 221: PASSED (0.30s)
| RESULTS - date.DateTest.test_date - Testcase 211: PASSED (0.99s)
| RESULTS - df.DfTest.test_df - Testcase 234: PASSED (0.28s)
| RESULTS - gi.GObjectIntrospectionTest.test_python - Testcase -1: SKIPPED (0.00s)
| RESULTS - oe_syslog.SyslogTest.test_syslog_running - Testcase 201: PASSED (0.28s)
| RESULTS - oe_syslog.SyslogTestConfig.test_syslog_logger - Testcase 1149: PASSED (0.51s)
| RESULTS - oe_syslog.SyslogTestConfig.test_syslog_restart - Testcase 1150: PASSED (0.41s)
| RESULTS - oe_syslog.SyslogTestConfig.test_syslog_startup_config - Testcase 202: PASSED (1.56s)
| RESULTS - opkg.OpkgRepoTest.test_opkg_install_from_repo - Testcase -1: PASSED (7.24s)
| RESULTS - parselogs.ParseLogsTest.test_parselogs - Testcase 1059: FAILED (3.43s)
| RESULTS - ping.PingTest.test_ping - Testcase 964: PASSED (0.11s)
| RESULTS - pttest.PttestRunnerTest.test_pttestrunner - Testcase 1600: SKIPPED (0.25s)
| RESULTS - scp.ScpTest.test_scp_file - Testcase 220: PASSED (1.44s)
| RESULTS - ssh.SSHTest.test_ssh - Testcase 224: PASSED (0.70s)
| RESULTS - xorg.XorgTest.test_xorg_running - Testcase 1151: FAILED (0.58s)
| SUMMARY:
| core-image-sato () - Ran 16 tests in 18.664s
| core-image-sato - FAIL - Required tests failed (skipped=2)
| ERROR: core-image-sato - FAILED - check the task log and the ssh log
| DEBUG: Python function do_testimage finished
| ERROR: Function failed: do_testimage
|
| Stdout:
| Machine information:
| *****
| Machine name: qemuriscv64
| CPU:
| Arch: riscv64
| Physical cores:
| Logical cores: 0
| *****
```


Buildroot

- <https://github.com/riscv/riscv-buildroot>
- Use 'riscv-start' branch
- Submitted Upstream
 - <http://lists.busybox.net/pipermail/buildroot/2018-September/230689.html>
- RV32 port
 - Submitted



Ongoing Effort

- RISC-V LLVM
- <https://github.com/lowRISC/riscv-llvm>
 - Experimental support is up-streamed
 - Full patch-set upstreaming is going on
 - LLD port has been submitted

Ongoing Effort

- Musl C library support
- <https://github.com/riscv/riscv-musl>
- Upstream submission Under Review
 - <https://www.openwall.com/lists/musl/2018/09/28/1>



Ongoing Effort

- OpenOCD
 - Out of tree <http://github.com/riscv/riscv-openocd>
 - Multi-core, 64-bit
- GDB (Linux)

Ongoing Effort

- UEFI
- Grub
- V8
- Node.js
- Rust

Contributions

- Unique Contributors to Linux arch ports (4.18)
 - X86 - 1908
 - ARM - 3053
 - MIPS - 906
 - PPC - 1462
 - **RISCV - 31** --> We need to get this number up

Find out more !!!

- Latest Software Status
 - <https://riscv.org/software-status/>
- Cores and SOC's overview
 - <https://riscv.org/risc-v-cores/>
- Mailing List
 - linux-riscv@lists.infradead.org

Get Involved

- Standards work (ABI, spec etc.)
- Improve/upstream Linux distribution support
- Port more software packages to RISC-V
- **Most Software is Upstream!**
 - Use a project's regular communication mechanisms
- **Specific to RISC-V**
 - <https://github.com/riscv/>: Contains in-progress ports
 - sw-dev@groups.riscv.org: Software discussion
 - patches@groups.riscv.org: Patches to RISC-V ports
 - #riscv on Freenode: General RISC-V discussion
 - linux-riscv@lists.infradead.org: RISC-V Linux Port
- **Stack Overflow**
 - <https://stackoverflow.com/questions/tagged/riscv>

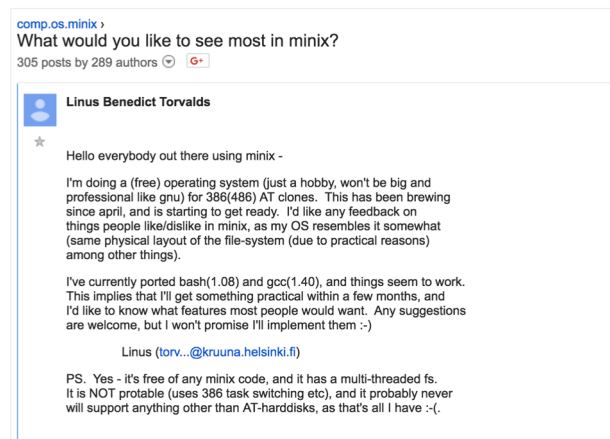
More on RISC-V @ ELCE 2018

Monday, October 22 • 18:00 - 18:40

BoF: RISC-V SW Ecosystem Status and Needs - Atish Patra, Western Digital; Olof Johansson, Palmer Dabbelt & Paul Walmsley, RISC-V

Seeds of Change (Some 25+ years ago)

- <https://groups.google.com/forum/#!msg/comp.os.minix/dlNtH7RRrGA/SwRavCzVE7gJ>
- 22M+ Lines of Code
- 14K+ contributors
- Unprecedented Development Velocity
- Most Successful Open Source Software Project



History Tends to repeat 😊

Usually when forgotten

But sometimes to build upon proven ways



Thank you

Khem Raj <raj.khem@gmail.com>



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